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(54) Single event upset hardening of commercial VLSI technology without circuit redesign.

(57) A fabrication method whereby any commercial integrated circuit design can be made SEU hardened simply by the fabrication process. No circuit redesign is required nor is circuit performance degraded. The novel method employs fully depleted accumulated mode type transistors on a silicon-on-insulator substrate. Modified LDD fabrication techniques are employed.

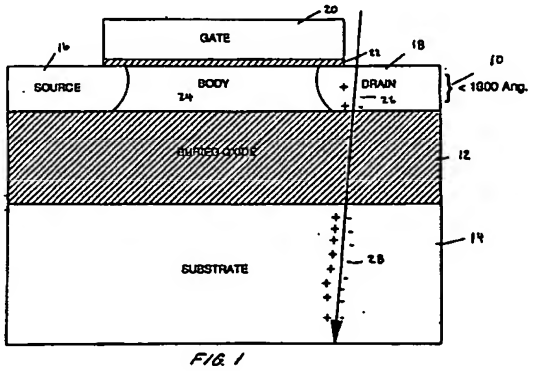

FIG. 1

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BACKGROUND OF THE INVENTION

1. Field of the Invention

This Invention relates to VLSI circuits and more particularly to radiation hardening of VLSI circuits without redesign.

2. Background of the Invention

Satellite-based integrated circuits are under constant ombardment from the very high energy particles and photons that are found in the outer atmosphere and in space. When impacting an integrated circuit, these particles can generate a local error, known as a single event upset (SEU). Additionally, as VLSI circuits increase in complexity and transistors sizes are reduced, even earth-bound integrated circuits are susceptible to SEU from background sources.

Typically, circuits are hardened against SEU by redesign such that the transistor diffusion areas are much larger thereby increasing the amount of capacitance that must be discharged in order to cause an upset and/or adding resistors to slow down any transient response. While effective in increasing SEU resistance, redesigning of circuits has certain drawbacks. These drawbacks include a loss in circuit speed, particularly with resistors operating at low temperatures and a loss of circuit density. Most importantly, the cost of redesigning a commercial chip set can be very expensive.

The manufacturing of semiconductor integrated circuits is an expensive and very competitive business. This is particularly true for the space product applications business, where relatively low volumes prohibit economies of scale. As a result,it is necessary to reduce costs without reducing quality. A large portion of the cost of producing very large scale integrated circuits (VLSI) is in the design of the chips. Thus, whenever possible, it is desirable to use existing design libraries. In general, this is the object of designing radiation hardened chips, where non-hardened designs are modified so as to meet the specifications required for a particular application. Still, even in this example, modifying the commercial design to comply with the SEU hardness expected in space products adds a significant cost to the product. In addition, circuit speed can be lost when resistors are added or when the original circuit design rules must be relaxed. Thus, a technology approach that eliminates the need for a redesign would add significant cost and performance savings in SEU hardened Integrated circuits.

As commercial technology moves to ever smaller devices, memory cells are becoming increasingly susceptible to SEU upset simply from background radiation. Thus, an improvement in the SEU hardness of commercial technology is desirable.

Though an object of the present invention is to present a fabrication method whereby any commercial circuit can be taken and become SEU hardened simply by the fabrication process. No circuit redesign is required, nor is circuit performance degraded.

Summary of the Invention

The invention is based on fabricating commercial VLSI circuit designs on fully depleted, accumulation mode devices using SOI substrates. With SOI, the circuits are fabricated in a very thin silicon layer which is situated on top a buried oxide layer. The basic advantages of SOI are well understood. SEU happens when a highly energetic particle strikes the drain diffusion region of an important transistor. As it traverses the silicon film, the particles generate a very large number of electron-hole pairs. The excess carriers that escape recombination are collected by the drain. A sufficient charge is collected by the drain, and the drain discharges its initial charge. With conventional bulk silicon, the cross sectional area for collecting charge is essentially the depth of the N-Well, which is typically two micrometer. Using SOI, the depth of the active area is reduced to the thickness of the silicon film or on the order of < 0.1 micrometer. Thus, to the first order, hardness is achieved by reducing the amount of device silicon in the path of energetic particles.

A second requirement of the invention is the use of fully depleted devices. While SOI can be used to meet very high prompt dose requirements, previous integrated circuit designs have used partially depleted devices. Partially depleted devices have a thicker silicon film, and hence the body of the transistor is not depleted of carriers when off. To meet SEU hardness requirements, partially depleted devices require shorting strap from the transistor body to the source and/or special ground contacts to the body of the transistor. Thus, partially depleted SOI devices are not compatible with bulk integrated circuit designs.

Another requirement of the present invention is that accumulation mode devices be used. In accumulation mode devices, the N-Channel (P-Channel) devices are comprised of n+ (p+) source and drain and n- (p-) body, and p+ (n+) doped polysilicon gates.

In a conventional transistor, the body is the opposite dopant type of the source and drain. The accumulation mode device is used in order to maintain design compatibility with bulk silicon without performance degradation. When conventional

transistor designs are implemented in bulk silicon, a very high body doping density must be used to achieve a bulk-like threshold voltage. This high doping density degrades the device performance parameters.

An optional embodiment of the present invention is the use of device engineering to increase the circuit power supply voltage to acceptable levels. At high power supply voltages, SOI circuits tend to have high standby leakage due to high electric field effects at the transistor level. By implementing conventional lightly doped drains as well as neutral impurity implants, high power supply voltages can be used. The device engineering part of the invention can be omitted for low voltage applications.

Brief Description of the Drawings

Figure 1 is a sketch of an SOI structure showing enhanced SEU resistance.

Figure 2 is a table comparing bulk, enhancement mode and accumulation mode device characteristics.

Figures 3 through 6 show the processing steps of the present invention.

Figure 7 is a graph showing the results of radiation testing of devices made according to the present invention.

Detailed Description of the Invention

Figure 1 is a sketch of an SOI structure showing enhanced SEU resistance. The silicon-on-insulator structure has a silicon layer 10 of a thickness of 85 nm. This silicon layer is formed upon a buried oxide layer 12 which is situated on a substrate 14 which may be silicon or other carrier wafer for supporting the silicon-on-insulator layers. Into this SOI structure a transistor is formed having source region 16, drain region 18, gate 20 with a gate oxide 22. A channel region of the device is formed in the body 24. Because of the reduced cross sectional area, a charge particle can only generate charge through the 10 device region picking up very little charge as shown 26 before the particle goes through the buried insulating oxide and into the substrate which, can create additional charges 28 but these charges 28 will not have an effect on a transistor device because of the intervening buried oxide layer 12.

A comparison of bulk, enhancement, and accumulation device types is shown in Figure 2. It can be seen that in order to achieve bulk like threshold voltages, the enhancement mode technology suffers from reduced transconductance and mobility. Also, not shown is the great sensitivity of enhancement devices to dopant concentration and film thickness.

The start of the fabrication process flow to hardening commercial VLSI circuits against single event upset is shown in Figure 3. Shown in Figure 3a is a substrate 30, buried oxide 32, silicon layer 34, which has a pad oxide 36 and a nitride layer 38 with a photo defined region 40. The etched pad stack to open areas where isolation is to be grown is shown in Figure 3b wherein isolation regions 42 are formed between the nitride etched pad stack. Once the local oxidation on the order of 240 - 300 nm 42 is grown, the pad oxide 36 and nitride layer 38 are stripped away.

A sacrificial oxidation on the order of 40 - 80 nm is grown on the silicon region 34 and stripped away to eliminate any stress induced damage from the pad stack. An extra optional photo level may be used to etch alignment marks into the substrate.

Shown in Figure 4a, is the next step which has a thin oxide growing on it as a sacrificial oxide for ion implantation. Next, a blanket implantation of a neutral impurity ions shown as 46 is blanket implanted over the entire surface of the wafer. Then ina photolithographic step, photo-resist 48 is covered over the n - channel areas and a p - channel threshold adjustment implant 50 is performed in the p - channel region (Figure 4b). Succeeding, the p - channel areas are covered with photo-resist 52 and an implant 54 is done to set the threshold voltage for the n type dopant (Figure 4c). The resist is removed and the sacrificial oxide 44 is removed.

Gate oxide is grown over the p and n channel regions as shown in Figure 5a. This gate oxide 56 is the final gate oxide. Covering the gate oxide is a deposition of polysilicon 58 which is used to form the gate electrode material. A very thin oxide is grown on the polysilicon layer to protect the polysilicon. The n-channel areas are covered with resist 60 and the polysilicon for the p-channel devices is doped with phosphorous implant ions 62. Next, the resist from the n-channel region is removed and resist 64 is coated over the p-channel region with ion implantation 66 of boron (Figure 5b). If boron ions are used, then to minimize the boron penetration from the p+ poly into the device, 10 kV boron should be implanted, rather than the usual boron difluoride (BF2) implant.

A nitride cap 68 is deposited over the entire surface of the wafer (Figure 5c). This nitride cap has a thickness of approximately 115 nm and is used to enhance the slope of the polysilicon gate during its etching and to protect the polysilicon doping from being changed during the diffusion implants.

Once the preceding steps are completed, further typical process steps are performed to complete the actual devices. This is done by defining

as shown in Figure 6a, the polysilicon gate where the poly is to be etched using photoresist, and proceeding to etchback the gate stack down to (but not including) the gate oxide. With the polysilicon gates defined an LDD implant can be formed in both the p-channel devices as shown in 6a and performing a low dose LDD implant on the n-channel devices using an n type dopant. Next, the n-channel devices can be coated with resist to form a light doped drain (LDD) implant on the p-channel devices using a p type dopant (Figure 6b). Next, silicon nitride can be deposited and etched back in an anisotropic etch to form a nitride implant spacer 72 (Figure 6c). With the implant spacer, the p-channel devices are covered with the resist and the high dose diffusion implant on n-channel devices is performed using a n type dopant (Figure 6d). This is followed by an anneal to activate the dopants and reduce implant damage. Next, the n- channel devices are coated with resist and the integrated circuit implanted with a high dose diffusion implant on the p-channel devices using a p type dopant (Figure 6e). This is annealed to activate the dopant and reduce implant damage. Then the nitride spacer and nitride cap are stripped with hot phosphoric acid (Figure 6f).

Upon completion of the devices, a final spacer and salicide formation in the source drain regions in the back end of the line processing can be completed to form the metalized devices. In the process flow it is assumed that all photoresist are stripped off immediately after the following etch or implant step.

The device definition stage listed above is strictly for the example of LOCOS isolation process described. The critical steps for forming fully depleted accumulation mode devices with device engineering are contained in the stages after device definition. Thus, the use of a different isolation scheme, that is trench, mesa, or other, does not constitute a separate invention. The LDD implant/spacer sequence is optional, and is only required to meet leakage requirements for higher power supply voltages and shorter gate lengths. Depending upon the gate length and/or power supply requirements, the LDD implant on both the n - and p - channel transistors can be varied or eliminated.

An example of operation as in the above process has built fully functional 256k SRAMs on multiple lots. Testing of these has resulted in radiation hardness as shown in Figure 7, showing an upset rate less than 1E-10 errors/bit*day. This upset level meets military and space product specifications.

Claims

1. A method of forming radiation hardened circuits from non- radiation hardened circuit designs comprising the steps of:
implementing the non-radiation hardened circuit designs in a silicon-on-insulator structure;
processing the silicon-on-insulator structures using semiconductor processing techniques to form fully depleted transistors; and
forming the transistors to operate as accumulation mode devices.

2. The method of Claim 1 wherein the transistors are formed using a lightly doped drain structure.

3. The method of Claim 1 wherein the circuits on formed on a silicon-on-insulator structure having a silicon thickness less than 0.1 micrometer.

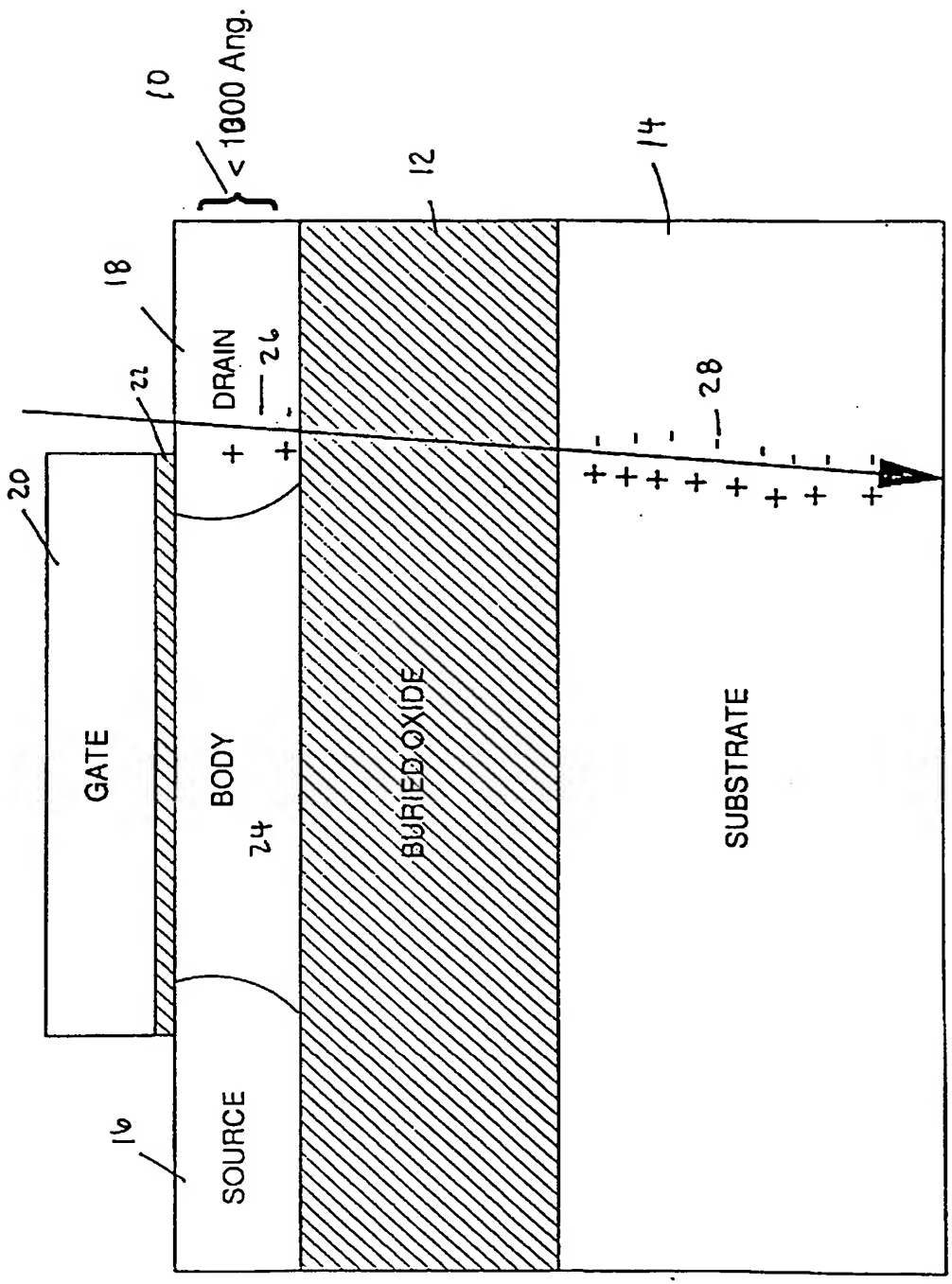
10
< 1000 Ang.
12
14
18
DRAIN
26
22
28
20
GATE
BODY
24
BURIED OXIDE
SUBSTRATE
16
SOURCE

FIG. 1

Parameter	Bulk CMOS	Enhancement Mode SOI	Accumulation Mode SOI	
N-Channel:				
Vt	0.80	0.65	0.83	Volts
sub Vt Slope	83	89	76	mV/dec.
Mobility	402	343	532	cm^2/V-sec
Gm (saturation)	110	92	120	uS/um
P-Channel:				
Vt	-0.60	-0.67	-0.70	Volts
sub Vt Slope	90	68	74	mV/dec.
Mobility	142	111	204	cm^2/V-sec
Gm (saturation)	60	48	62	uS/um

FIG. 2

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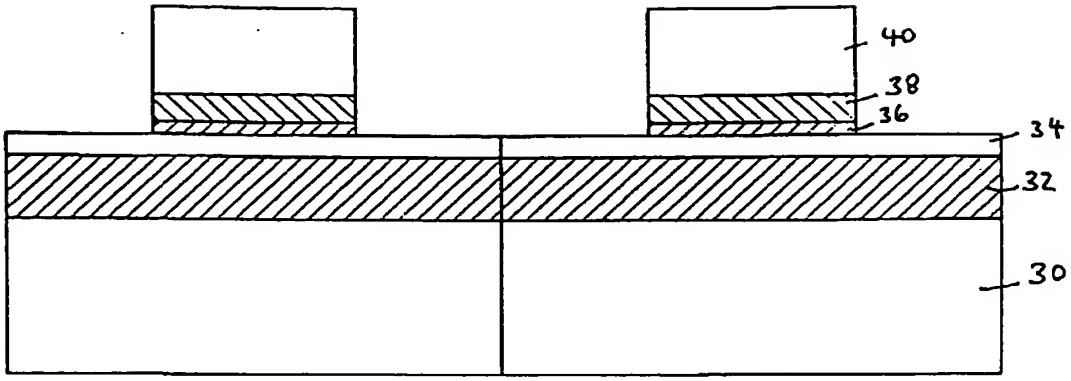

FIG.3 (a)

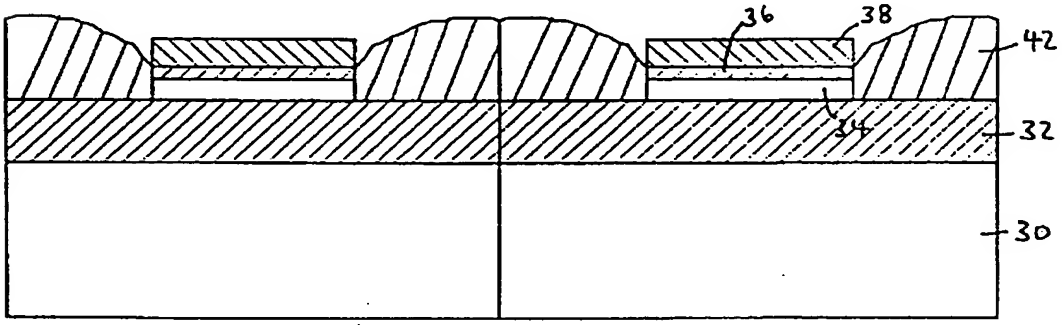

FIG.3 (b)

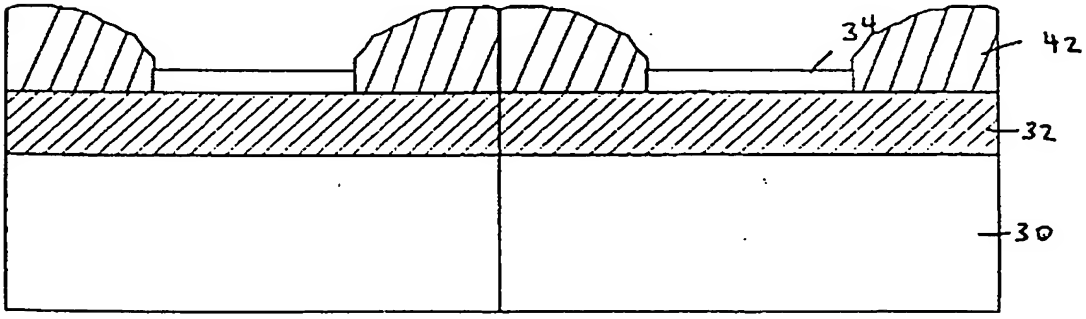

FIG. 3 (c)

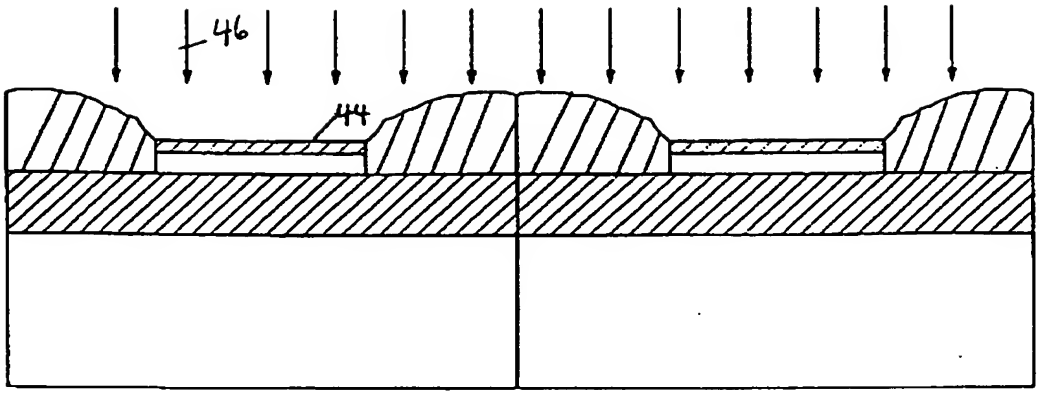

FIG. 4 (a)

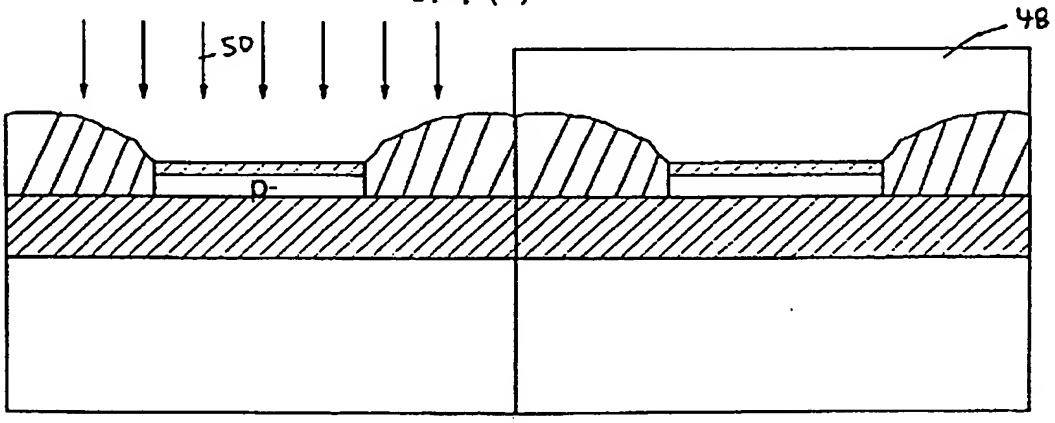

FIG. 4 (b)

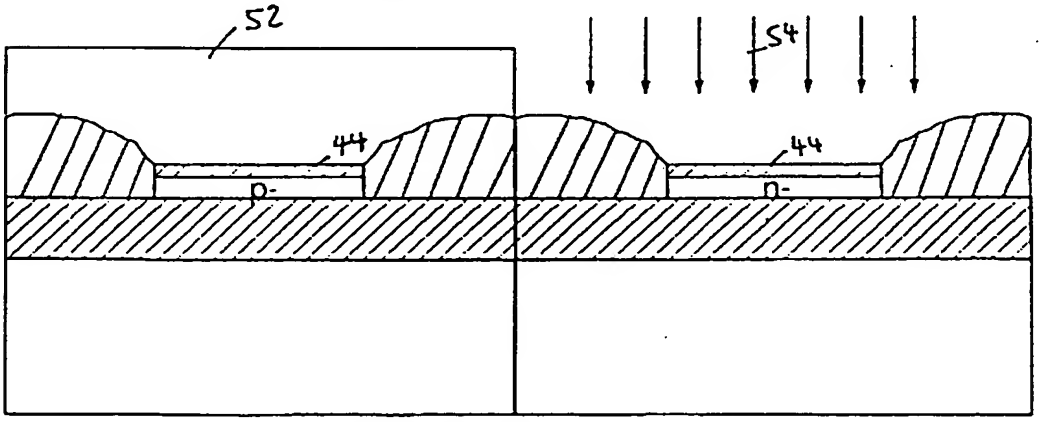

FIG. 4 (c)

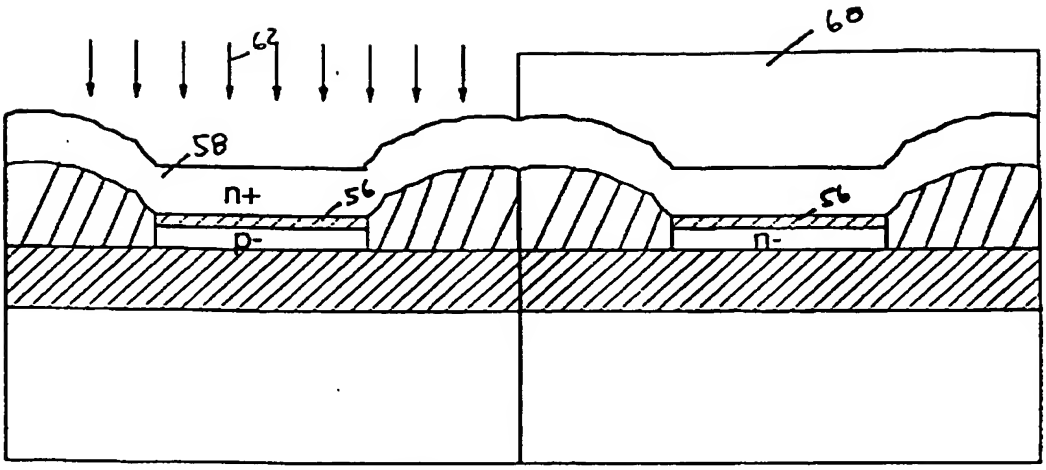

FIG. 5 (a)

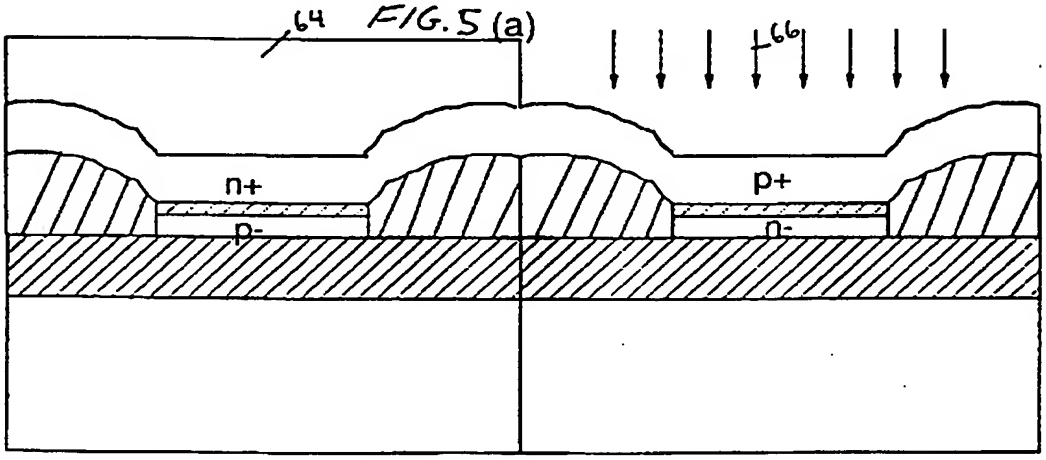

FIG. 5 (b)

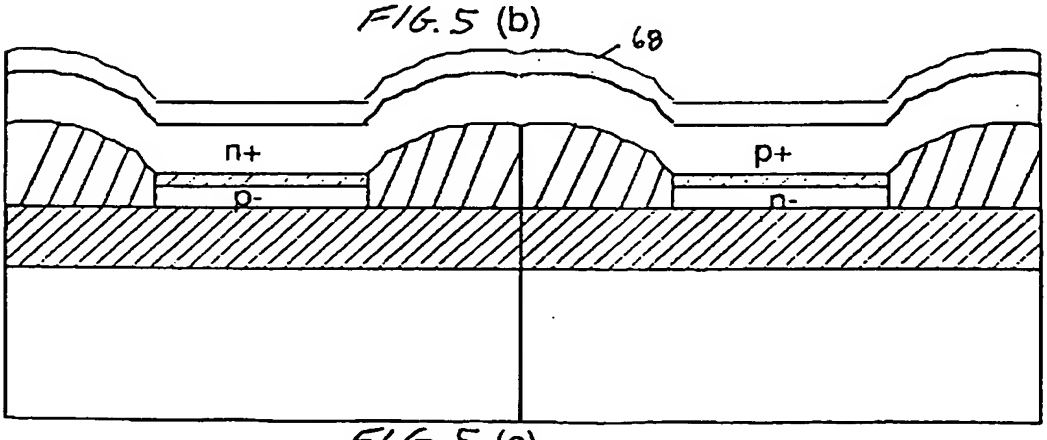

FIG. 5 (c)

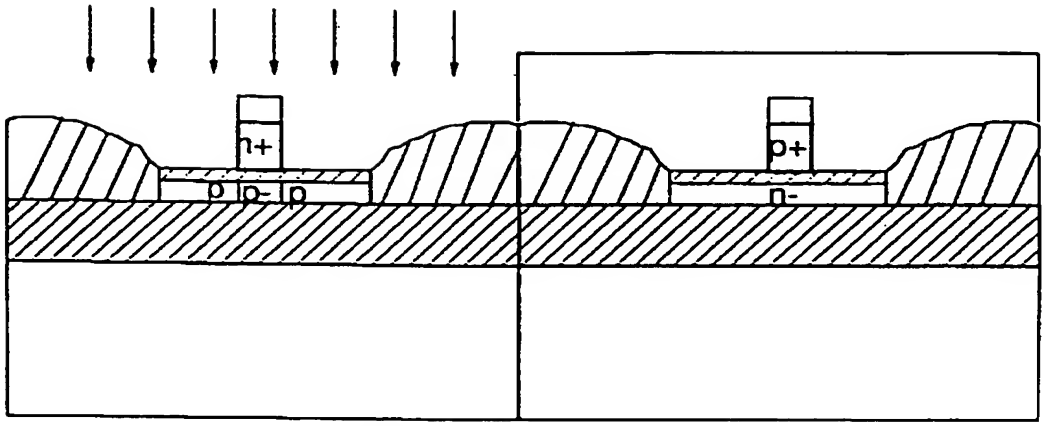

FIG. 6 (a)

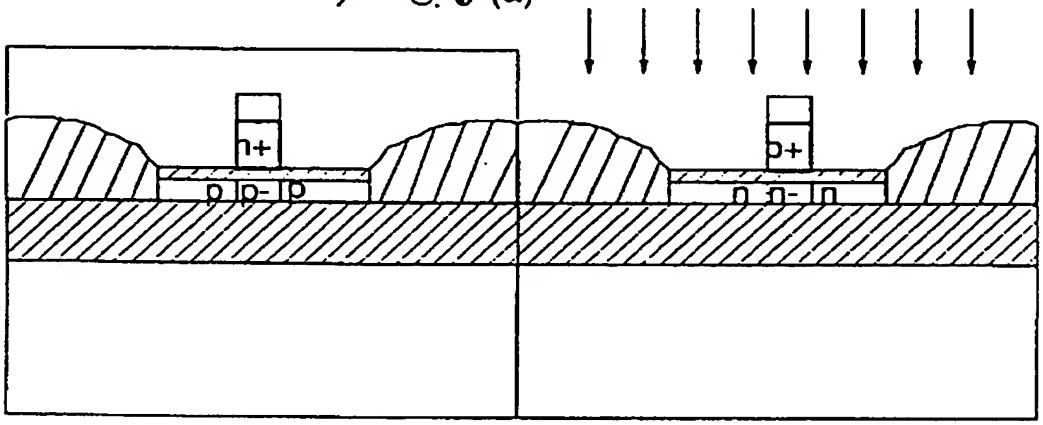

FIG. 6 (b)

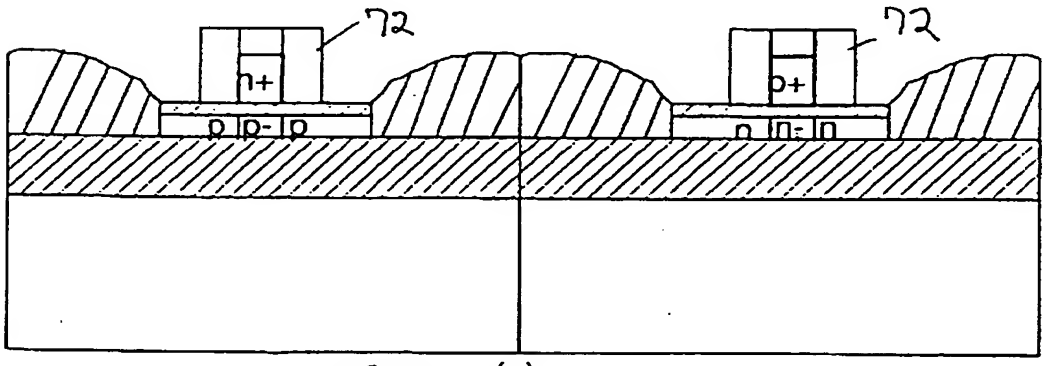

FIG. 6 (c)

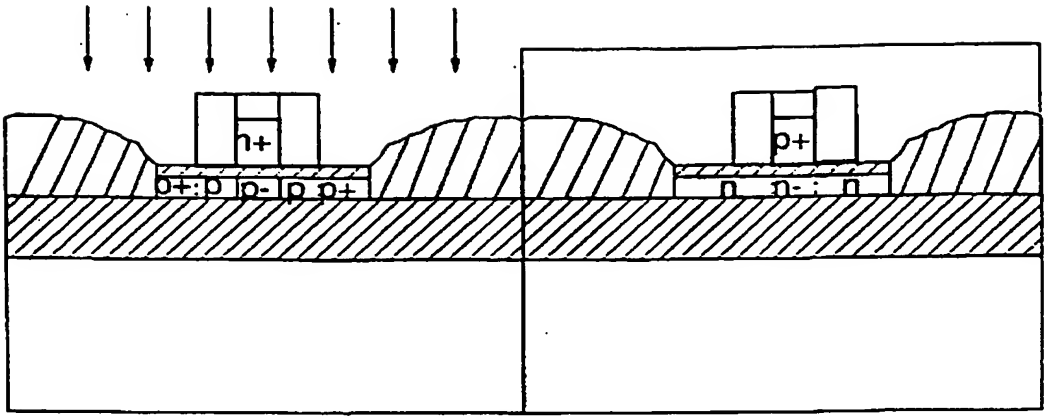

FIG. 6 (d)

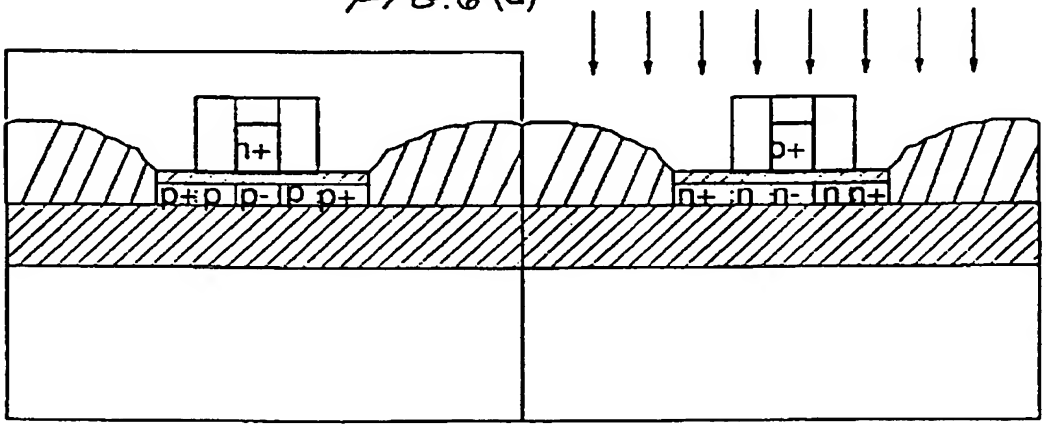

FIG. 6 (e)

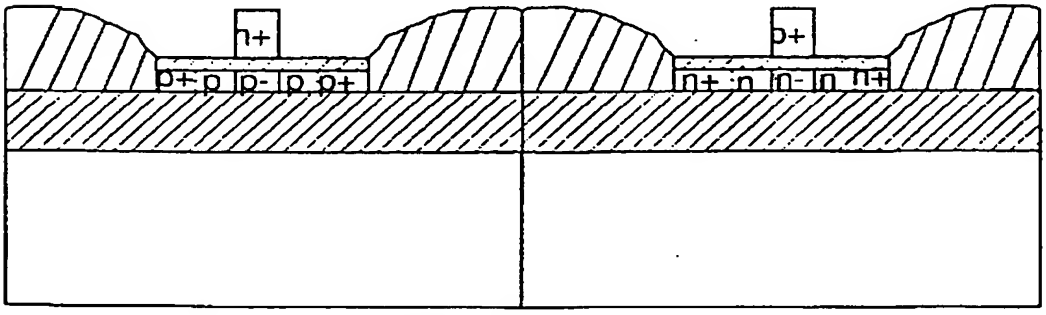

FIG. 6 (f)

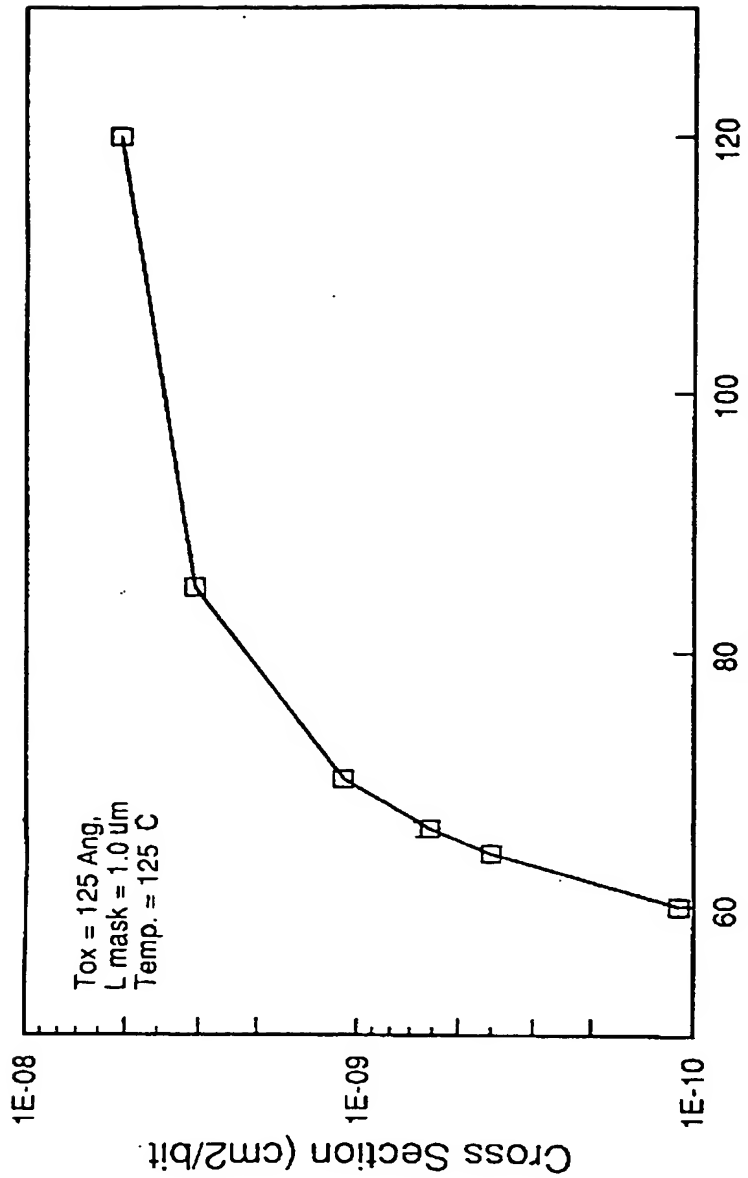
Cross Section (cm2/bit
1E-08
1E-09
1E-10
60
80
100
120
LET (MeV-cm2/mg)
Tox = 125 Ang,
L mask = 1.0 um
Temp. = 125 C

FIG. 7

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 94 11 3502

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	IEEE TRANSACTIONS ON ELECTRON DEVICES, vol.39, no.3, March 1992, NEW YORK US pages 640 - 647 A. KAMGAR ET AL * paragraph I-III * ---	1-3	H01L21/84 H01L29/78 H01L23/552
A	US-A-4 091 527 (A. M. GOODMAN ET AL) * column 3, line 59 - column 6, line 30; figures 5-22 * ---	1-3	
A	US-A-5 104 818 (J. SILVER) * the whole document * ---	1,2	
A	EP-A-0 474 289 (N.V. PHILIPS' GLOEILAMPENFABRIEKEN) * figure 1; example 1 * -----	1-3	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
BERLIN	10 February 1995	Roussel, A

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
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E : earlier patent document, but published on, or after the filing date
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